CLAIMS

What is claimed is:

1. A semiconductor device package comprising:

a lead frame including a die paddle and a plurality of lead fingers;

a first semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the first semiconductor die is electrically coupled to at least one lead finger of the plurality of lead fingers; and

a second semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a second size different from the first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die is electrically coupled to the at least one lead finger and, wherein the second semiconductor die exhibits circuitry substantially identical in function to circuitry of the first semiconductor die.

2. The semiconductor device package of claim 1, further comprising an amount of insulating material encapsulating the first semiconductor die, the second semiconductor die, the die paddle and a portion of each of the plurality of lead fingers.

3. The semiconductor device package of claim 1, wherein the die paddle exhibits a peripheral outline which is smaller than a peripheral outline of the first semiconductor die.

4. The semiconductor device package of claim 1, wherein the at least one bond pad of the first semiconductor die corresponds in location on its respective semiconductor die with the at least one bond pad of the second semiconductor die and wherein the at least one bond pad of the first semiconductor die and the at least one bond pad of the second semiconductor die are electrically connected with a common lead finger of the plurality of lead fingers.

5. The semiconductor device package of claim 1, further comprising a volume of dielectric material encapsulating the first semiconductor die, the second semiconductor die, the die paddle and a portion of each of the plurality of lead fingers.

6. The semiconductor device package of claim 1, wherein at least one of the first semiconductor die and the second semiconductor die is adhered to the die paddle with a thermally conductive material.

7. The semiconductor device package of claim 1, wherein the lead frame further comprises at least one tie bar coupled with the die paddle and wherein the at least one tie bar is configured and located so as to pass through a stay out zone, remaining clear of any electrical interconnection between the plurality of bond pads of the first semiconductor die and the plurality of lead fingers.

8. The semiconductor device package of claim 1, further comprising at least one alignment feature formed in the lead frame.

9. The semiconductor device package of claim 8, wherein the at least one alignment feature is formed in at least one tie bar of the lead frame.

10. The semiconductor device package of claim 1, wherein the second semiconductor die is adhered to the die paddle along at least a portion of an active surface of the second semiconductor die paddle.

11. The semiconductor device package of claim 10, wherein the first size is smaller than the second size.

12. The semiconductor device package of claim 11, wherein the first semiconductor die includes an active surface and an opposing surface and wherein the first semiconductor die is adhered to the die paddle along at least a portion of the opposing surface.

13. The semiconductor device package of claim 1, wherein the die paddle exhibits a peripheral outline which is smaller than a peripheral outline of the first semiconductor die.

14. A memory device comprising:

a carrier substrate;

a plurality of electrical contacts coupled with electrical circuitry formed in the carrier substrate; and

at least one semiconductor device package coupled with the electrical circuitry in the carrier substrate, the at least one semiconductor device package comprising:

a lead frame including a die paddle and a plurality of lead fingers;

a first semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the first semiconductor die is electrically coupled to at least one lead finger of the plurality of lead fingers; and

a second semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a second size different from the first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die is electrically coupled to the at least one lead finger and, wherein the second semiconductor die exhibits circuitry substantially identical in function to circuitry of the first semiconductor die.

15. The memory device of claim 14, wherein the at least one bond pad of the first semiconductor die corresponds in location on its respective semiconductor die with the at least one bond pad of the second semiconductor die and wherein the at least one bond pad of the first semiconductor die and the at least one bond pad of the second semiconductor die are electrically connected with a common lead finger of the plurality of lead fingers.

16. The memory device of claim 14, wherein at least one of the first semiconductor die and the second semiconductor die is adhered to the die paddle with a thermally conductive material.

17. The memory device of claim 14, wherein the second semiconductor die is adhered to the die paddle along at least a portion of an active surface of the second semiconductor die paddle.

18. The memory device of claim 17, wherein the first size is smaller than the second size.

19. The memory device of claim 18, wherein the first semiconductor die includes an active surface and an opposing surface and wherein the first semiconductor die is adhered to the die paddle along at least a portion of the opposing surface.

20. A computing system comprising:

a carrier substrate;

a processor operably coupled to the carrier substrate;

at least one input device operably coupled with the carrier substrate;

at least one output device operably coupled with the carrier substrate; and

a memory device operably coupled to the carrier substrate, the memory device including at least one semiconductor device package, the at least one semiconductor device package comprising:

a lead frame including a die paddle and a plurality of lead fingers;

a first semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the first semiconductor die is electrically coupled to at least one lead finger of the plurality of lead fingers; and

a second semiconductor die adhered to the die paddle, the first semiconductor die exhibiting a second size different from the first size and having a plurality of bond pads, wherein at least one bond pad of the plurality of bond pads of the second semiconductor die is electrically coupled to the at least one lead finger and, wherein the second semiconductor die exhibits circuitry substantially identical in function to circuitry of the first semiconductor die.

21. The computing system of claim 20, wherein the at least one bond pad of the first semiconductor die corresponds in location on its respective semiconductor die with the at least one bond pad of the second semiconductor die and wherein the at least one bond pad of the first semiconductor die and the at least one bond pad of the second semiconductor die are electrically connected with a common lead finger of the plurality of lead fingers.

22. The computing system of claim 20, wherein at least one of the first semiconductor die and the second semiconductor die is adhered to the die paddle with a thermally conductive material.

23. The computing system of claim 20, wherein the second semiconductor die is adhered to the die paddle along at least a portion of an active surface of the second semiconductor die paddle.

24. The computing system of claim 23, wherein the first size is smaller than the second size.

25. The computing system of claim 24, wherein the first semiconductor die includes an active surface and an opposing surface and wherein the first semiconductor die is adhered to the die paddle along at least a portion of the opposing surface.

26. A method of forming a semiconductor device package, the method comprising:
providing a lead frame having a die paddle and a plurality of lead fingers;
providing a first semiconductor device exhibiting a first size;
adhering a surface of the first semiconductor die to the die paddle;
electrically connecting at least one of a plurality of bond pads formed on the first semiconductor die to a first lead finger of the plurality of lead fingers;
providing a second semiconductor device exhibiting a second size different from the first size and configuring circuitry of the second semiconductor die to be substantially identical in function to circuitry of the first semiconductor die;
adhering a of active surface of a second semiconductor die to an upper side of the die paddle; and
electrically connecting at least one of a plurality of bond pads formed on the active surface of the second semiconductor die to a second lead finger of the plurality of lead fingers.

27. The method according to claim 26, further comprising encapsulating the first semiconductor die, the second semiconductor die, the die paddle and a portion of each of the plurality of lead fingers with a dielectric material.

28. The method according to claim 26, further comprising forming the die paddle with a peripheral outline which is smaller than a peripheral outline of the first semiconductor die.

29. The method according to claim 26, further comprising forming at least one alignment mark in a portion of the lead frame.

30. The method according to claim 26, wherein adhering the active surface of the first semiconductor die further includes disposing a thermally conductive material between the active surface of the first semiconductor die and the die paddle.